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APPLICATION FOR LETTERS PATENT

for

SORTING A GROUP OF INTEGRATED CIRCUIT DEVICES FOR THOSE DEVICES REQUIRING SPECIAL TESTING

Inventor:
Raymond J. Beffa

Attorney:
James R. Duzan
Registration No. 28,393
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
(801) 532-1922

TITLE OF THE INVENTION

SORTING A GROUP OF INTEGRATED CIRCUIT DEVICES FOR THOSE DEVICES REQUIRING SPECIAL TESTING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of application Serial No. 10/379,257, filed March 3, 2003, pending, which is a continuation of application Serial No. 09/607,201, filed June 28, 2000, now U.S. Patent 6,529,793, issued March 4, 2003, which is a continuation of application Serial No. 09/145,758, filed September 2, 1998, now U.S. Patent 6,122,563, issued September 19, 2000, which is a continuation of application Serial No. 08/801,565, filed February 17, 1997, now U.S. Patent 5,844,803, issued December 1, 1998, which is related to: a co-pending application having Serial No. 08/591,238, entitled "METHOD AND APARATUS [sic] FOR STORAGE OF TEST RESULTS WITHIN AN INTEGRATED CIRCUIT," and filed January 17, 1996; a co-pending application having Serial No. 08/664,109, entitled "A STRUCTURE AND A METHOD FOR STORING INFORMATION IN A SEMICONDUCTOR DEVICE," and filed June 13, 1996, now U.S. Patent 5,895,962, issued April 20, 1999; an application having Serial No. 08/785,353, entitled "METHOD FOR SORTING INTEGRATED CIRCUIT DEVICES," and filed January 17, 1997, now U.S. Patent 5,927,512, issued July 27, 1999; a co-pending application having Serial No. 08/822,731, entitled "METHOD FOR CONTINUOUS, NON LOT-BASED INTEGRATED CIRCUIT MANUFACTURING," and filed March 24, 1997, now U.S. Patent 5,856,923, issued January 5, 1999; a co-pending application having Serial No. 08/806,442, entitled "METHOD IN AN INTEGRATED CIRCUIT (IC) MANUFACTURING PROCESS FOR IDENTIFYING AND RE-DIRECTING IC'S [sic] MIS-PROCESSED DURING THEIR MANUFACTURE," and filed February 26, 1997, now U.S. Patent 5,915,231, issued June 22, 1999; and a co-pending application having Serial No. 08/871,015, entitled "METHOD FOR USING DATA REGARDING MANUFACTURING PROCEDURES INTEGRATED CIRCUITS (IC'S) [sic] HAVE UNDERGONE, SUCH AS REPAIRS, TO SELECT PROCEDURES THE IC'S [sic] WILL UNDERGO, SUCH AS

ADDITIONAL REPAIRS," and filed June 6, 1997, now U.S. Patent 5,907,492, issued May 25, 1999.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: The present invention relates in general to integrated circuit (IC) manufacturing and, more specifically, to methods in IC manufacturing processes for sorting IC devices using identification (ID) codes, such as fuse IDs, in the devices.

[0003] State of the Art: Integrated circuits (ICs) are small electronic circuits formed on the surface of a wafer of semiconductor material, such as silicon, in an IC manufacturing process referred to as "fabrication." Once fabricated, ICs are electronically probed to evaluate a variety of their electronic characteristics, cut from the wafer on which they were formed into discrete IC dice or "chips," and then assembled for customer use using various well-known IC packaging techniques, including lead frame packaging, Chip-On-Board (COB) packaging, and flip-chip packaging.

[0004] Before being shipped to customers, packaged ICs are generally tested to ensure they will function properly once shipped. Testing typically involves a variety of known test steps, such as pre-grade, burn-in, and final, which test ICs for defects and functionality and grade ICs for speed.

[0005] As shown in FIG. 1, a variety of data are collected as ICs proceed through an IC manufacturing process. For example, fabrication deviation data reflecting quality deviations, such as fabrication process errors, are collected during fabrication and summarized in one or more reports commonly referred to as "Quality Deviation Reports" (QDRs). Similarly, data are collected during probe which record the various electronic characteristics of the ICs tested during probe.

[0006] When any of the wafers in a wafer lot are deemed to be unreliable because they are low yielding wafers, as indicated by the collected probe data, or because they are misprocessed wafers, as indicated by the QDRs, all the ICs from the wafers in the wafer lot typically undergo special testing, such as enhanced reliability testing, that is more extensive and strict than standard testing. Since a wafer lot typically consists of fifty or more wafers, many ICs

that undergo the special testing do not require it because they come from wafers that are not deemed unreliable. Performing special testing on ICs that do not need it is inefficient because such testing is typically more time-consuming and uses more resources than standard testing. Therefore, there is a need in the art for a method of identifying those ICs in a wafer lot that require special testing and sorting the ICs in the wafer lot into those that require special testing and those that do not.

[0007] As described in U.S. Patent Nos. 5,301,143, 5,294,812, and 5,103,166, some methods have been devised to electronically identify individual ICs. Such methods take place "off" the manufacturing line, and involve the use of electrically retrievable identification (ID) codes, such as so-called "fuse IDs," programmed into individual ICs to identify the ICs. The programming of a fuse ID typically involves selectively blowing an arrangement of fuses and anti-fuses in an IC so that when the fuses or anti-fuses are accessed, they output a selected ID code. Unfortunately, none of these methods addresses the problem of identifying and sorting ICs "on" a manufacturing line.

BRIEF SUMMARY OF THE INVENTION

[0008] An inventive method in an integrated circuit (IC) manufacturing process for sorting IC devices of the type having an identification (ID) code, such as a fuse ID, into those devices requiring a first testing process, such as enhanced reliability testing, and those devices requiring a second testing process, such as standard testing, includes storing data in association with the ID code of each of the devices that indicates each of the devices requires the first or the second testing process. The data may include fabrication deviation data, such as a Quality Deviation Report (QDR), probe data, standard test data, or special test data, such as enhanced reliability testing data. Also, the data may, for example, indicate the need for the first or second testing process by indicating that one or more semiconductor wafers or wafer lots have been misprocessed, or have relatively low yields at probe or during testing. Further, the data may be generated by IC devices other than those devices to be sorted, and may be generated at a point in the manufacturing process before or after the point at which sorting will take place.

[0009] The ID code of each of the IC devices to be sorted is automatically read. This may be accomplished, for example, by electrically retrieving a unique fuse ID programmed into each of the devices, or by optically reading a unique laser fuse ID programmed into each of the devices. Also, the data stored in association with the automatically read ID code of each of the IC devices is accessed, and the devices are then sorted in accordance with the accessed data into those devices requiring the first testing process and those devices requiring the second testing process.

[0010] The present invention thus provides a method that directs those ICs needing enhanced reliability testing to such testing without the need for all ICs from the same wafer lot, including those from reliable wafers, to proceed through special testing.

[0011] In additional embodiments, the method described above is included in methods for manufacturing IC devices and Multi-Chip Modules (MCMs) from semiconductor wafers.

[0012] In a further embodiment, an inventive sorting method uses special test data generated by a first group of IC devices undergoing special testing to sort a second group of devices of the type having an identification (ID) code, such as a fuse ID, into those devices requiring the special testing and those requiring standard testing. Specifically, the method includes storing data in association with the ID code of some of the IC devices in the second group that indicates the devices require special testing. Special test data generated by the first group of devices is then stored in association with the ID codes of the previously mentioned devices in the second group, and the special test data indicates these devices in the second group that were previously indicated to require special testing instead require only standard testing. The ID codes of these devices in the second group are then automatically read, the data stored in association with the ID codes is accessed, and the second group of devices is sorted in accordance with the accessed data so the appropriate devices in the second group undergo standard testing.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0013] FIG. 1 is a flow diagram illustrating a conventional procedure in an integrated circuit (IC) manufacturing process for directing ICs to special testing, such as enhanced reliability testing; and

[0014] FIG. 2 is a flow diagram illustrating a procedure in an IC manufacturing process for directing ICs to special testing, such as enhanced reliability testing, in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] As shown in FIG. 2, an inventive method 10 for manufacturing integrated circuits (ICs) from a group of semiconductor wafers in a wafer lot 12 includes the step 14 of fabricating the ICs on the wafers. Any fabrication process errors occurring during the fabrication step 14 are noted in a Quality Deviation Report (QDR) 16. It will be understood by those having skill in the field of this invention that the present invention is applicable to any IC devices, including Dynamic Random Access Memory (DRAM) ICs, Static Random Access Memory (SRAM) ICs, Synchronous DRAM (SDRAM) ICs, processor ICs, Single In-line Memory Modules (SIMMs), Dual In-line Memory Modules (DIMMs), and other Multi-Chip Modules (MCMs).

[0016] After fabrication, the ICs are electronically probed in a probe step 18 to evaluate a variety of their electronic characteristics, and data from the probe step 18 are noted and stored as probe data 16. The probe data 16 may include, for example, data indicating that one or more wafers are providing a relatively low yield of ICs that are functional at probe, or data indicating that an abnormal number of problems are associated with wafers from a particular wafer lot, or with ICs from the same position on a series of wafers, or with ICs processed by a particular piece of fabrication equipment.

[0017] Before, during, or after the probe step 18, ICs fabricated on the wafers are programmed in a program step 20 in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID for each IC is then stored as data in association with the QDR/probe data 16 for that IC. The fuse ID may identify, for example, a wafer lot ID, the week

the ICs were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. It will be understood, of course, that the present invention includes within its scope ICs having any ID code, including those having fuse IDs. It will also be understood that the ID code for each IC need not be unique, but instead may only specify the wafer the IC comes from, for example.

[0018] Once programmed, the ICs proceed through an assembly step 22 and then to a sort step 24. At this point in the manufacturing process, QDR/probe data 16 is available not only for those ICs presently at the sort step 24, but also for those ICs trailing the ICs presently at the sort step 24 which have completed the probe step 18. Therefore, sufficient QDR/probe data 16 may exist to determine that a particular wafer, for example, is unreliable as a result of low yields from the wafer at the probe step 18, or as a result of a processing error at the fabrication step 14. Similarly, sufficient QDR/probe data 16 may exist to determine that wafers from a particular wafer lot are unreliable, or that ICs from a particular location on a series of wafers are unreliable, or that ICs processed by a particular piece of fabrication equipment are unreliable.

[0019] As noted above, ICs that are deemed to be unreliable typically require some form of special testing, such as enhanced reliability testing, in which testing standards and methods are more strict than standard testing. Therefore, at the sort step 24, the fuse IDs of the ICs are automatically read so the QDR/probe data 16 (and test data 26, 28, and 30 as described below) stored in association with the fuse IDs may be accessed and used to sort the ICs into those ICs requiring special testing in a special test step 32, and those ICs requiring only standard testing in one or more test steps 34 and 36. It should be understood that although the fuse IDs are typically read electronically, they may also be read optically if the fuse ID consists of "blown" laser fuses that are optically accessible.

[0020] In general, the test data 26, 28, and 30 comprise data generated by ICs at one point in the IC manufacturing process which is used to sort ICs under test at a different point in the process. Thus, for example, test data 26 and 28 generated by ICs from a particular wafer may indicate that the wafer is unreliable because of low yields during the test steps 34 and 36. As a result, ICs from the same wafer that have yet to be tested may be diverted at the sort step 24 to the special test step 32.

[0021] Similarly, test data 26 and 28 generated by ICs from a particular wafer lot, or by ICs from a particular die location on a series of wafers, or by ICs that were processed by a particular piece of fabrication equipment at the fabrication step 14, may indicate that ICs respectively from the same wafer lot, or from the same die location, or that were processed by the same piece of fabrication equipment, are unreliable because of low yields or other problems at the test steps 34 and 36. As a result, ICs respectively from the same wafer lot, or from the same die location, or that were processed by the same piece of fabrication equipment, that have yet to be tested may be diverted at the sort step 24 to the special test step 32.

[0022] Likewise, test data 30 generated by ICs deemed unreliable and tested in the special test step 32 may indicate that similarly situated ICs that have yet to be tested are not, in fact, unreliable, and therefore need not be diverted to the special test step 32. The test data 26, 28, and 30 will be described in more detail below.

[0023] Thus, the present invention provides a method 10 that directs those ICs needing special testing to the special testing step 32 without the need for all ICs from the wafer lot 12, including those from reliable wafers, to proceed through the special testing step 32. In addition, because the method 10 takes advantage of test data 26 and 28 generated by already tested ICs to sort yet-to-be-tested ICs, the method 10 advantageously provides real-time feedback of data back up the manufacturing line. Further, because the method 10 takes advantage of QDR/probe data 16 generated by ICs trailing ICs presently at the sort step 24 to sort those ICs presently at the sort step 24, the method 10 advantageously provides real-time feedback of data down the manufacturing line.

[0024] Those ICs that proceed on to the standard test step 34 are tested in a variety of well-known ways so the test data 26 may be generated and stored for each IC in association with the fuse ID of the IC. It should be understood that the test step 34 may comprise many individual test procedures, or just one. It should also be understood that the test data 26 may include data such as the following: data identifying the testing equipment that tested the ICs, operating personnel who operated the testing equipment, and the set-up of the equipment when the ICs were tested; and data indicating the time and date the ICs were tested, the yield of shippable ICs through the test step 34, and test results for the ICs from the various stages of the test step 34.

[0025] The ICs tested in the test step 34 then proceed on to an intra-test sort step 38, where the fuse ICs of the tested ICs are again automatically read so the ICs can be sorted in accordance with the QDR/probe data 16, the test data 26, and the test data 28 and 30 of other previously tested ICs, into those ICs requiring special testing in the special test step 32, and those ICs eligible to continue with standard testing in the test step 36.

[0026] At the intra-test sort step 38, the QDR/probe data 16 and test data 26, 28, and 30 may identify those ICs in need of special testing in the same manner as described above with respect to the sort step 24. In addition, the test data 26 and 28 may indicate that ICs that were tested by a particular piece of test equipment at the test step 34 are unreliable because of low yields or other problems at the test steps 34 and 36. As a result, ICs that were processed by the same piece of test equipment may be diverted at the sort step 38 to the special test step 32.

[0027] Of course, it should be understood that the special test procedures conducted on ICs sorted out in the intra-test sort step 38 may differ from those conducted on ICs sorted out in the sort step 24. Also, it should be understood that the present invention includes within its scope those methods which include only a pre-test sort step, such as the sort step 24, or only an intra-test sort step, such as the sort step 38, or any combination thereof.

[0028] Those ICs that continue on to the standard test step 36 are also tested in a variety of well-known ways so the test data 28 may be generated and stored for each IC in association with the fuse ID of the IC. It should be understood that the test step 36 may comprise many individual test procedures, or just one. It should also be understood that the test data 28 may include data such as the following: data identifying the testing equipment that tested the ICs, operating personnel who operated the testing equipment, and the set-up of the equipment when the ICs were tested; and data indicating the time and date the ICs were tested, the yield of shippable ICs through the test step 36, and test results for the ICs from the various stages of the test step 36.

[0029] The ICs tested in the test step 36 then proceed on to a post-test sort step 40, where the fuse IDs of the tested ICs are yet again automatically read so the ICs can be sorted in accordance with the QDR/probe data 16, the test data 26 and 28, and the test data 30 of other

previously tested ICs, into those ICs requiring special testing in the special test step 32, and those ICs eligible to be shipped (the disposition of non-shippable ICs is not shown).

[0030] At the post-test sort step 40, the QDR/probe data 16 and test data 26, 28, and 30 may identify those ICs in need of special testing in the same manner as described above with respect to the sort steps 24 and 38. In addition, the test data 28 may indicate that ICs that were tested by a particular piece of test equipment at the test step 36 are unreliable because of low yields or other problems at the test step 36. As a result, ICs that were processed by the same piece of test equipment may be diverted at the sort step 40 to the special test step 32.

[0031] Of course, it should be understood that the special test procedures conducted on ICs sorted out in the post-test sort step 40 may differ from those conducted on ICs sorted out in the sort step 24 and the intra-test sort step 38. Also, it should be understood that the present invention includes within its scope those methods which include only a pre-test sort step, such as the sort step 24, only an intra-test sort step, such as the sort step 38, or only a post-test sort step, such as the sort step 40, or any combination thereof.

[0032] Those ICs that proceed on to the special test step 32 are subjected to a variety of special tests, such as enhanced reliability tests, so the test data 30 may be generated and stored for each IC in association with the fuse ID of the IC. It should be understood that the special test step 32 may comprise many individual test procedures, or just one. It should also be understood that the test data 30 may include data such as the following: data identifying the testing equipment that tested the ICs, operating personnel who operated the testing equipment, and the set-up of the equipment when the ICs were tested; and data indicating the time and date the ICs were tested, the yield of shippable ICs through the test step 32, and test results for the ICs from the various stages of the test step 32. Of course, those ICs that pass the special test step 32 are generally allowed to ship.

[0033] The present invention thus provides an inventive method for identifying those ICs in a wafer lot that require special testing through the use of ID codes, such as fuse IDs, and for sorting the ICs in the wafer lot into those that require special testing and those that do not using the ID codes of the ICs. The invention also advantageously provides real-time feedback of

data up and down the IC manufacturing line by using probe and test data generated by already probed or tested ICs to sort yet-to-be-tested ICs.

[0034] Although the present invention has been described with reference to a preferred embodiment, the invention is not limited to this embodiment. For example, while the various steps of the preferred embodiment have been described as occurring in a particular order, it will be understood that these steps need not necessarily occur in the described order to fall within the scope of the present invention. Thus, the invention is limited only by the appended claims, which include within their scope all equivalent methods that operate according to the principles of the invention as described.